

40V, 500mA Single Channel High Power Linear LED Driver**Features**

- ★ Adjustable output current LED driver
- ★ Support digital and analog dimming control
- ★ Maximum 500mA output current regulator
- ★ Wide supply voltage ranges from 4.5V to 40V
- ★ $\pm 4\%$ output current accuracy
- ★ Low quiescent current
- ★ Thermal protect: Current ramp down $3.3\%/^{\circ}\text{C}$
- ★ RoHS Compliant and Halogen Free

General Description

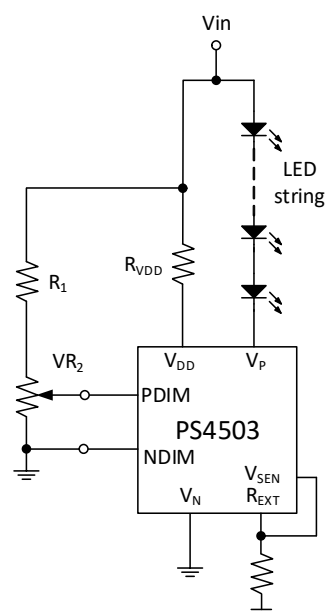
PS4503 is a single channel LED driver with adjustable output current. The output current typically ranges from 20mA to 500mA through external current setting resistor (R_{EXT}). To achieve no flick feature with analog dimming control, the set output current is linearly controlled by dimming control (PDIM pin) ranging from 0.25V to 3V. However, digital dimming control is obtained by giving PWM signal to dimming control (PDIM pin).

PS4503 offers excellent output current accuracy with supply voltage (V_{DD}) from 4.5V to 40V and output voltage (V_{PN}) up to 40V. PS4503 is featured a thermal protection by output current ramp down ($3.3\%/^{\circ}\text{C}$) as junction temperature is located from 130°C to 150°C . Moreover, taking reliability into consideration, the absolute maximum voltage rating (AMR) on V_{DD} and OUT is designed as 45V ability to handle high voltage pulse suddenly.

PS4503 is available in the cost-effective package PSOP-8.

Applications

- ★ Bus/Train walk way lighting
- ★ Indoor healthy lighting
- ★ Class room lighting
- ★ RGB pixel light bar

Basic Application Circuit

Contents

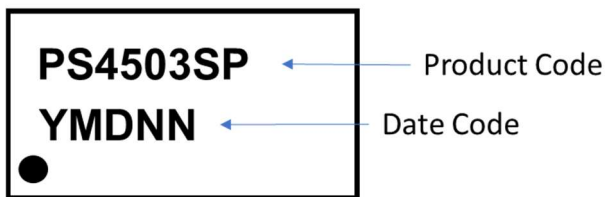
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1 Ordering Information

Part no.	Package	Description	Pin1 Orientation Follow EIA-481-D	Product code
PS4503SP	SP: PSOP-8 (Exposed Pad)	40V, 500mA Single Channel High Power Linear LED Driver	_1: Quadrant 1	PS4503SP

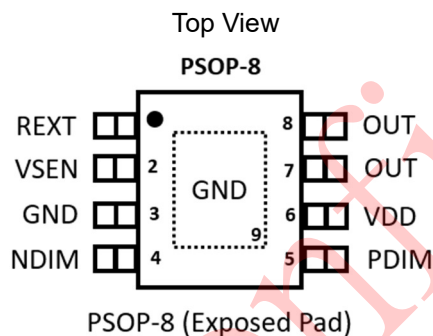
2 Marking Information

PSOP-8



3 Device Information

3.1 Pinout



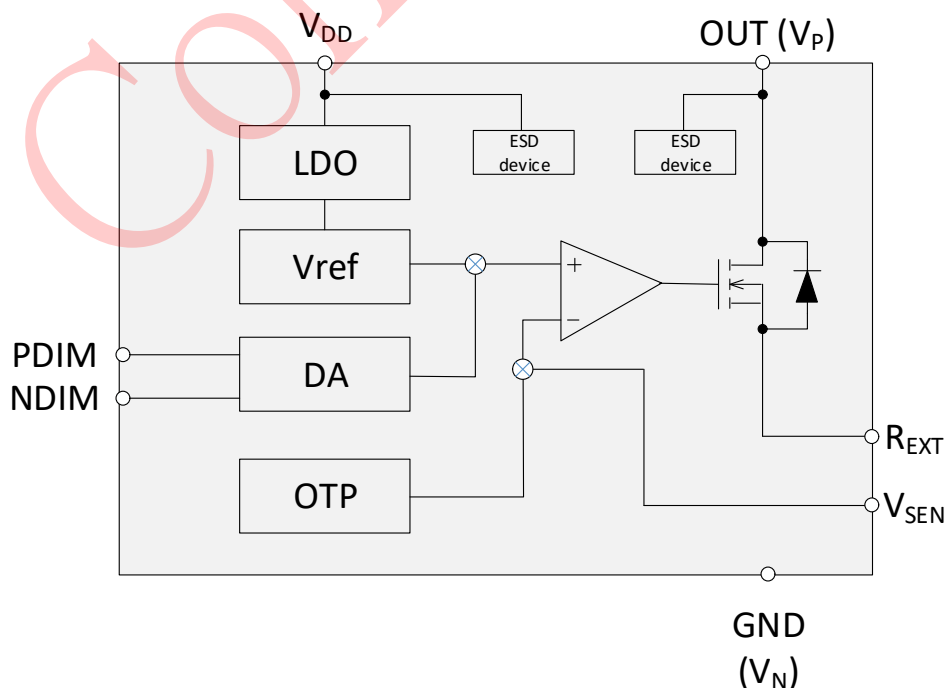
3.2 Pin Definitions and Functions

Pin	Name	I/O ⁽¹⁾	Descriptions
1	REXT	O	External current sense resistor output pin. This pin is internally connected to the source terminal of MOSFET and negative terminal of an operational amplifier. The voltage between REXT pin and GND(V_N) pin is controlled to 0.2V for full-scale output current. An external current setting resistor set this full-scale current. The distance between external current setting resistor and PS54503 should be as short as possible.
2	VSEN	I	Voltage sense input pin. Connect V_{SEN} pin to positive terminal of current sense resistor with independent trace for more accurate current regulation. Don't leave this pin floating.

3	GND(V_N)	--	Negative dimming current pin. This pin is also called power ground pin. For more accurate current regulation, connect this pin to negative terminal of current sense resistor with independent trace.
4	NDIM	I	Negative dimming control input pin. This pin is internally connected to negative terminal of differential amplifier for dimming control. Generally, connect this pin to the GND(V_N) pin.
5	PDIM	I	Positive dimming control input pin. This pin is initial pull-high as V_{DD} is ready. The voltage on PDIM pin presents 3V for full-scale dimming current if PDIM pin keeps floating. Moreover, the PDIM pin is internally connected to the positive terminal of differential amplifier for dimming control. The dimming command (V_{CMD}) is the voltage difference between PDIM pin and NDIM pin. V_{CMD} typically ranges from 0.2V to 3V for increasing dimming current from 6.7% to 100% full-scale current. V_{CMD} below 0.1V will shut down the output current.
6	VDD	I	Supply voltage input. V_{DD} is recommended from 4.5V to 40V.
7,8	OUT(V_P)	O	Regulated current sink pin. Dimming current flows into this pin and is regulated by V_{CMD} .

(1) I= Input, O= Output, --= Other

3.3 Functional Block Diagram



4 Specifications

4.1 Absolute Maximum Ratings ⁽¹⁾

Condition	MIN	MAX	Unit
V _{DD}	-0.2	45	V
V _{PN}	-0.2	45	
P _{DIM}	-5	7	
N _{DIM}	-5	7	
V _{SEN}	-0.2	5	
Operating Junction Temperature		150	°C
Storage Temperature Range	-65	150	

4.2 Thermal Information ⁽²⁾

Package Thermal Resistance		Unit
Junction to board thermal resistance (θ_{JA})	49	°C/W
Junction to case thermal resistance (θ_{JC})	15	

4.3 Power Dissipation

Item	Value	Unit
P _D @TA=25°C (PSOP-8)	2	W

4.4 Recommended Operating Conditions ⁽³⁾

Item	Value	Unit
V _{DD}	4.5 to 40	V
V _{PN}	P _{DMAX} / I _S	V
Operating Junction Temperature	-40 to 125	°C/W

- (1) Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- (2) θ_{JA} is measured with the component mounted on minimum pad PCB, θ_{JC} is measured at the exposed pad of the package.
- (3) Device function is not guaranteed if it is operated out of this recommended range.

4.5 Electrical Characteristic

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE & CURRENT						
Supply voltage	V_{DD}	$I_{PN} \leq 500\text{mA}$, no reverse protects	4.5	--	40	V
Supply current	I_{DD}	$4.5\text{V} \leq V_{DD} \leq 40\text{V}$, $I_{PN}=500\text{mA}$	0.1	0.2	0.4	mA
OUTPUT VOLTAGE & CURRENT & ACCURACY & LEAKAGE						
Output voltage	$V_{PN}^{(1)}$	$V_{DD} \geq 7\text{V}$, $I_{PN} = 500\text{mA}$	1	--	20	V
Output leakage	I_{LEAK}	$V_{DD} = 0\text{V}$, $V_{PN} = 36\text{V}$	--	0	5	μA
Output Current Sense Voltage	V_{REXT}	$V_{DD} \geq 4.5\text{V}$, $I_{PN}=I_S$	0.192	0.2	0.208	V
Output current accuracy	I_{ACY}	$V_{DD} \geq 4.5\text{V}$, $V_{CMD} \geq 1\text{V}$	-4	--	4	%
Output current vs V_{DD} regulation	I_{ACY_VDD}	$V_{PN}=1.1\text{V}$, $V_{DD}=4.5\text{V}\sim 40\text{V}$	-2	--	2	%
Output current vs V_{PN} regulation	$I_{ACY_VPN}^{(2)}$	$V_{DD}=4.5\text{V}$, $V_{PN}=1.1\text{V}\sim 36\text{V}$	-1	--	1	%
Maximum output current	$I_{S_MAX}^{(3)}$	$V_{DD} \geq 4.5\text{V}$, $R_{EXT} = 0.4\Omega$	480	500	520	mA
DROPOUT VOLTAGE						
Minimum dropout voltage	V_T	$I_{PN} > 95\% I_{S_MAX}^{(3)}$, $V_{DD} \geq 4.5\text{V}$	--	--	1	V
DIMMING COMMAND VOLTAGE						
Dimming command voltage	V_{CMD}	$V_{CMD} = V_{PDIM} - V_{NDIM}$	0	--	5	V
Max. input reference voltage	V_{NDIM_MAX}	$I_{ACY} \leq \pm 4\%$	-2	--	2	V
Input voltage (V_{CMD}) logic high	V_{IH}	$-2\text{V} \leq V_{NDIM} \leq 2\text{V}$	2.85	3	3.15	V
Input voltage (V_{CMD}) logic low	V_{IL}	$-0.3\text{V} \leq V_{NDIM} \leq 0.3\text{V}$	0.1	0.15	0.25	V
PDIM pull high current	I_{PDIM_H}	$V_{DD} \geq 4.5\text{V}$, $V_{PDIM} = 0\text{V}$	5	13	20	μA
THERMAL PROTECT						
OTP start temperature	T_{OTP}	$I_{PN} \geq 90\% I_S$	--	130	--	$^{\circ}\text{C}$
OTP output decreasing rate	T_{OTDR}	$T_J \geq T_{OTP}$	--	3.3	--	$\%^{\circ}\text{C}$

(1) V_{PN} tested in pulse mode.(2) I_{ACY_VPN} tested in pulse mode.(3) I_{S_MAX} is 500mA. I_S is defined as the full-scale output current, ranging from 10mA to 120mA, set by the REXT pin resistance. I_{PN} is actual output current, ranging from 0 to 100% I_S , regulated by V_{CMD} .

4.6 Switching Characteristic

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V _{DD} power on delay	t _{PrOnDly}	V _{PN} = 2V, V _{DD} = 0V → 7V	--	3	5	μs
V _{DD} power on rising	t _{PrOnRise}	PDIM floating, NDIM = 0V R _{EXT} = 0.4Ω, I _{PN} ≥ 90%I _S	--	4	7	
V _{DD} power off delay	t _{PrOffDly}	V _{PN} = 2V, V _{DD} = 7V → 0V	--	--	100	ns
V _{DD} power off falling	t _{PrOffFall}	PDIM floating, NDIM = 0V R _{EXT} = 0.4Ω, I _{PN} ≤ 10%I _S	--	--	400	
P _{DIM} switch on delay	t _{OEOnDly}	V _{PN} = 2V, V _{DD} = 7V	--	3	5	μs
P _{DIM} switch on rising	t _{OEOnRise}	V _{CMD} = 0V → 3.5V R _{EXT} = 0.4Ω, I _{PN} ≥ 90%I _S	--	4	7	
P _{DIM} switch off delay	t _{OEOffDly}	V _{PN} = 2V, V _{DD} = 7V	--	--	1000	ns
P _{DIM} switch off falling	t _{OEOffFall}	V _{CMD} = 3.5V → 0V R _{EXT} = 0.4Ω, I _{PN} ≤ 10%I _S	--	--	400	

4.7 Output current calculation

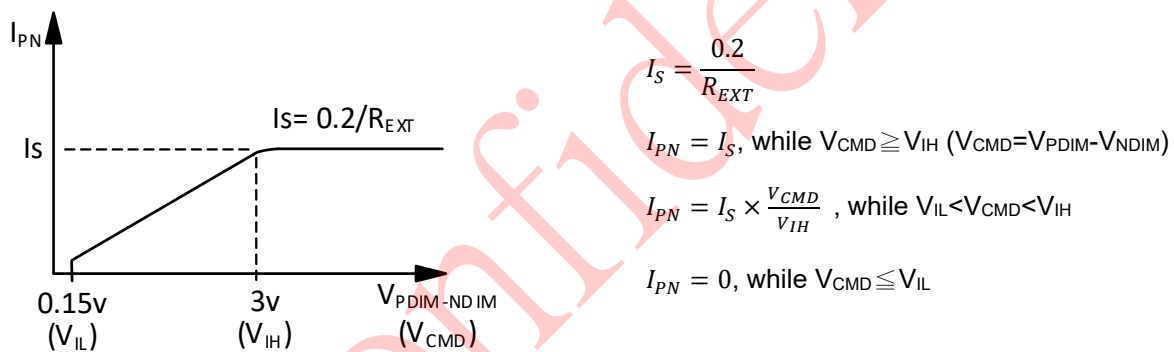


Figure 1. V_{CMD} VS. I_{OUT} curve.

4.8 Input pin equivalent circuit

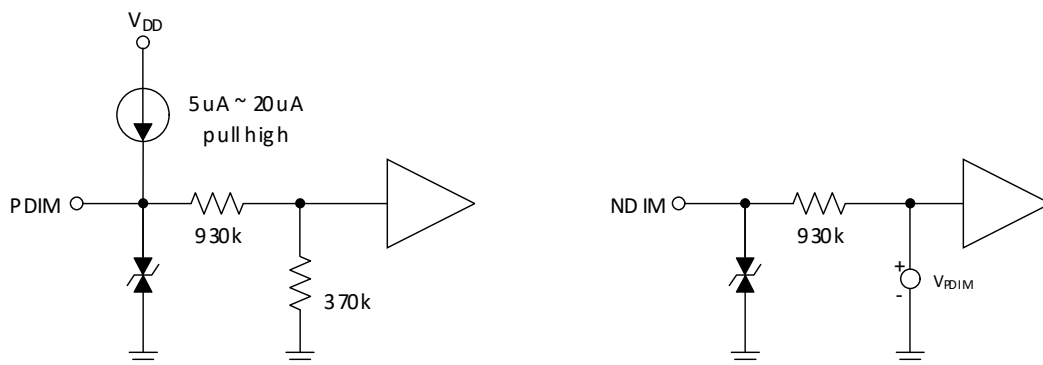


Figure 2. Input pin equivalent circuit.

4.9 Temperature VS IOOUT characteristic

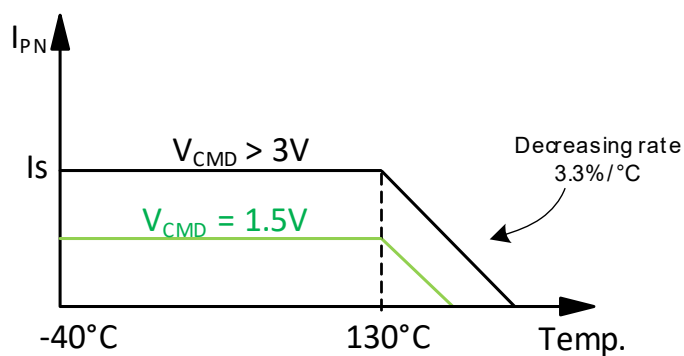


Figure 3. OTP characteristic

5 Typical Characteristics

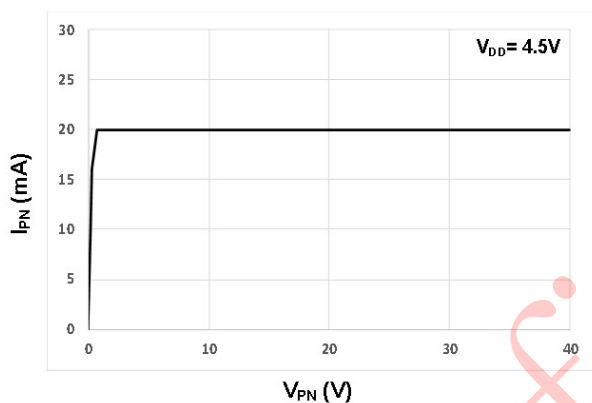


Figure 4. Load regulation, I_{PN} vs V_{PN}

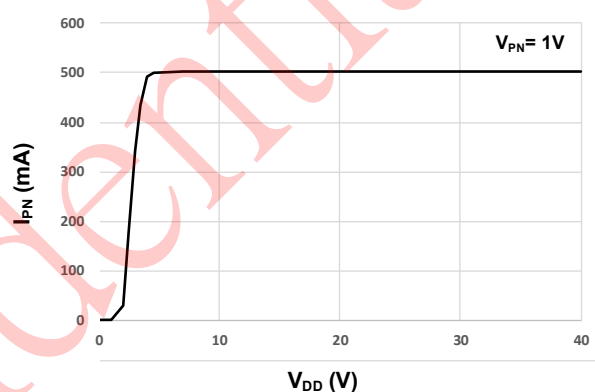


Figure 5. Line regulation, I_{PN} vs V_{DD}

6 Application Information

The PS4503 is a Constant Current Regulator (CCR) for LED driver. It is achieved by adjusting the internal self-biased transistor to regulate the current through PS4503 or any devices in series with it. Besides, as operating temperature rising, PS4503 features a thermal protection function to protect LEDs through reducing operating current if junction temperature of PS4503 is above 130°C.

6.1 Single LED String

PS4503 can be placed in a series of LEDs string, as shown in Figure 6. The number of the LEDs is limited by the voltage across the V_{PN} of PS4503 and V_{IN} supply voltage. Hence, the design must estimate the voltage across the LEDs and PS4503 by taking the minimum input voltage greater than the sum of maximum voltage across the LED string and minimum V_{PN} drop out.

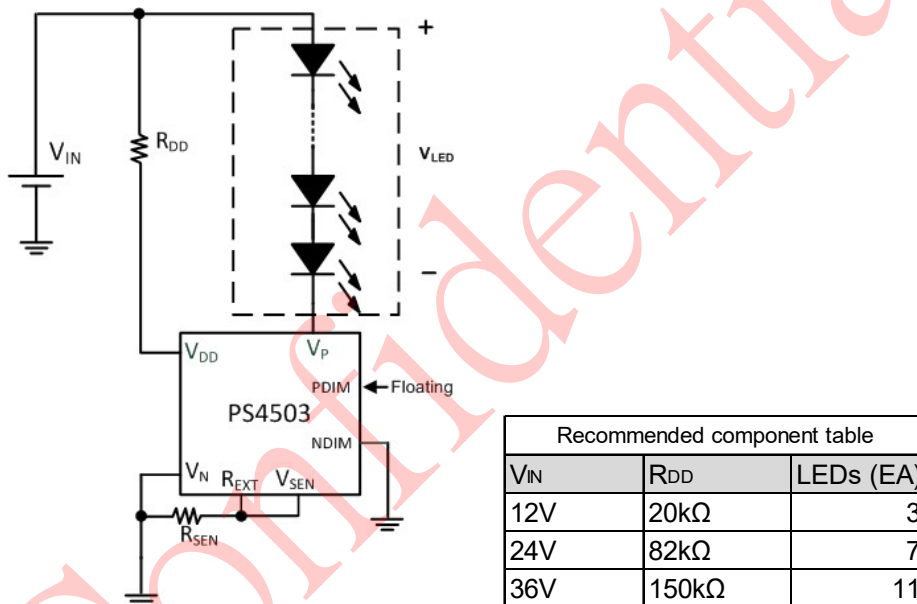


Figure 6. General LED driving application

Figure 6 is a general LED driving method. the minimum input voltage $V_{IN(min)}$ has to be higher than $V_{LED} + V_{PN}$ or $I_{DD} \cdot R_{DD} + 4.5V$. Resistor R_{DD} is used to protect the V_{DD} pin from damage due to fast V_{IN} transitions, such as hot plug of V_{IN} power or unexpected high spikes from power line. The equation is as follows:

$$V_{IN(min)} = V_{LED(max)} + V_{PN(min)} \quad (1)$$

$$R_{DD} \leq \frac{V_{IN} - 4.5V}{I_{DD(max)}} \quad (2)$$

Figure 7 shows another way to driving LEDs. In this way, the self-bias V_{DD} voltage of PS4503 is equal to the total V_F voltage of LEDs between V_{DD} and V_P pin plus $V_{PN(min)}$ voltage. This V_{DD} voltage should be approximately above 4.5V. Generally, 1 white LEDs or 2 red LEDs between V_{DD} and V_P pin are sufficient for this application.

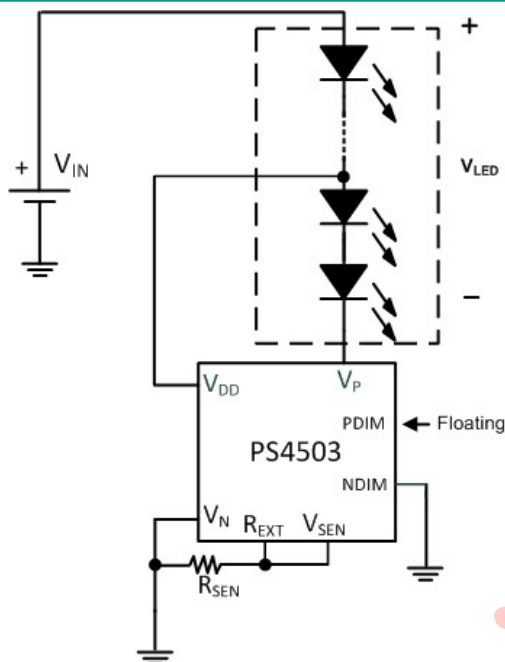


Figure 7. Self-bias LED driving application

6.2 Higher Current LED Strings

For higher LED current demand, two or more PS4503 can be connected in parallel to increase the LED current as shown in Figure 8.

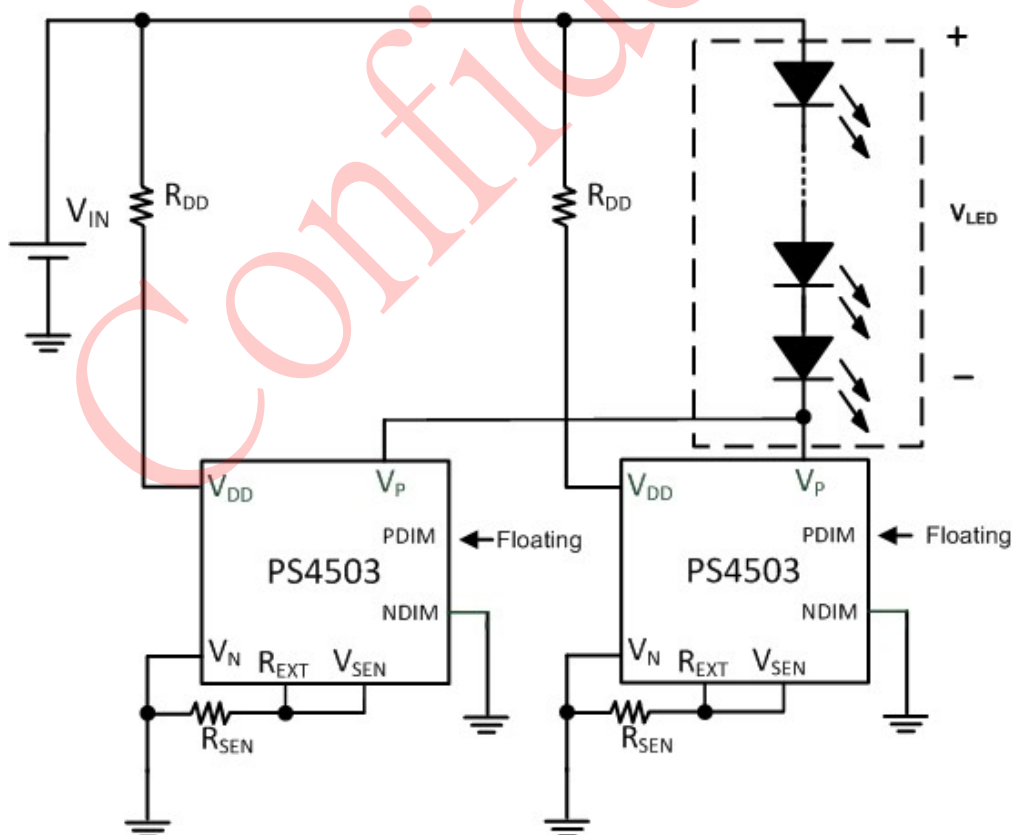


Figure 8. High current application.

6.3 PWM Dimming

Figure 9 is the best PWM dimming application circuit. To achieve LED dimming in an LED driving circuit with the PS4503, you can use a MOSFET to switch the power supply. The brightness is controlled by the duty cycle of a PWM (Pulse Width Modulation) signal. Resistor R_{DD} and R_{PL} act as a voltage divider to generate the proper V_{DD} voltage for PS4503 and discharge the residual charge on power line while the switch MOSFET is off. To discharge the residual charge is important because it will cause instability in dimming control, resulting in flickering or inconsistent brightness. The duty cycle of the PWM signal is defined as the ratio of the LED on time (T_{ON}) to the entire cycle time (T). The duty cycle of the PWM signal is shown in Figure 10. Figure 11 shows the current accuracy with different duty cycle.

$$Duty = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T} \quad \dots\dots\dots (3)$$

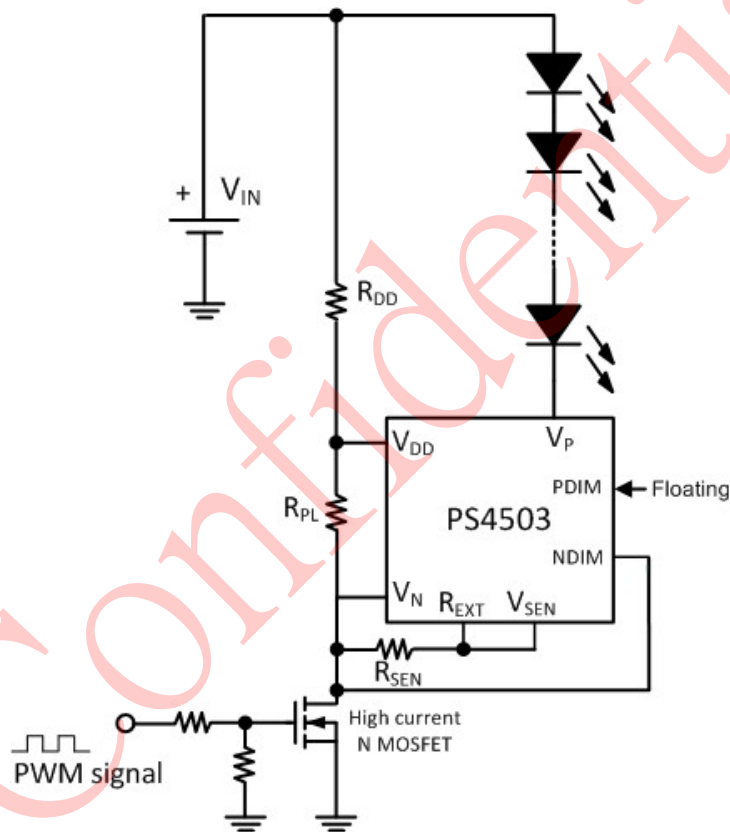


Figure 9. PWM dimming by external MOSFET

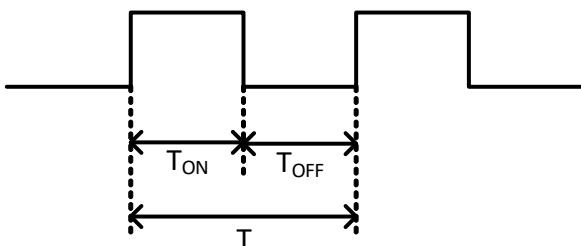


Figure 10. PWM dimming signal



Figure 11. Current accuracy vs PWM dimming

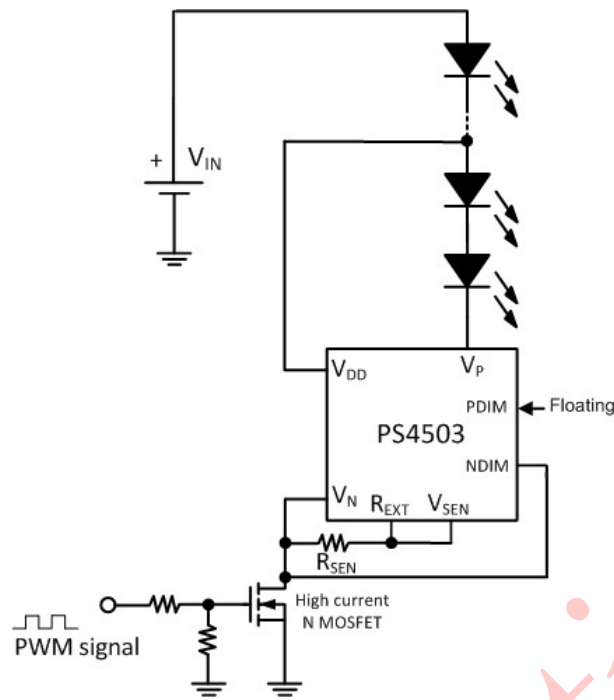


Figure 12. Simplified dimming circuit.

Figure 12 shows the self-bias dimming circuit. The advantage is no need of resistor for PS4503 biasing. In many compact LED applications this will mostly reduce the procedure of production. The disadvantage is the PWM dimming frequency should be lower. It is suggested the frequency should be lower than 1KHz to get better dimming control. Both switch N MOSFETs in Figure 9 and Figure 12 are to switch the total power of LED loads, so it should have lower R_{DS} resistance and larger power dissipation capability to minimize the power lost and heat generation. If a simpler PWM dimming method is used, the MCU can send a PWM signal (0~5V) through the GPIO pin to control the VDD ON-OFF time to achieve dimming purposes (Figure 13). Or the dimming function can be realized by sending a differential voltage signal of 0~3V through the PDIM and NDIM pins (see Figure 14).

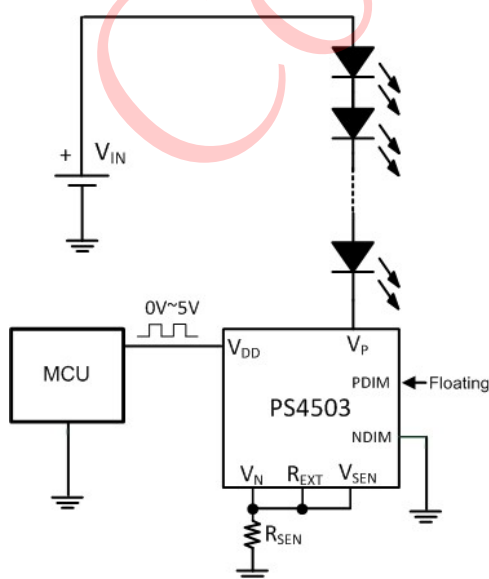


Figure 13. PWM dimming by MCU

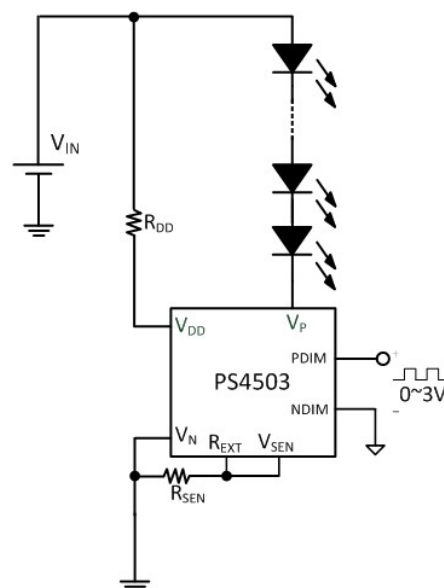


Figure 14. PWM dimming by PDIM and NDIM

6.4 Thermal Protection: LED Current Ramp Down

For protecting LED under high temperature application, LED current is decreased automatically while PS4503's junction temperature is over 130°C. Besides, if PS4503's junction temperature approaches 145°C, LED current remains around 10%. Along with temperature reducing, the LED current is recovery when junction temperature is below 130°C.

6.5 Power Dissipation

The power dissipation can be determined from the regulated current I_S multiplying the voltage across the V_{PN} that is the supply voltage on V_P to substrate the voltage across the LED string V_{LED} .

$$V_{PN} = V_{IN} - V_{LED} \quad \dots\dots\dots (3)$$

$$P_D = I_S \times V_{PN} \quad \dots\dots\dots (4)$$

As the power requirement of LED is increased, the power dissipation should be considered for thermal relief. The maximum power dissipation supported by the device is dependent on PCB layout design, PCB material and operating ambient temperature. Further, the maximum power dissipation before current ramp down function triggering is given by:

$$P_{D(max)} = \frac{130 - T_A}{R_{\theta JA}} \text{ , where } R_{\theta JA} = 49^\circ\text{C/W} \quad \dots\dots\dots (5)$$

7 Typical Application Circuit

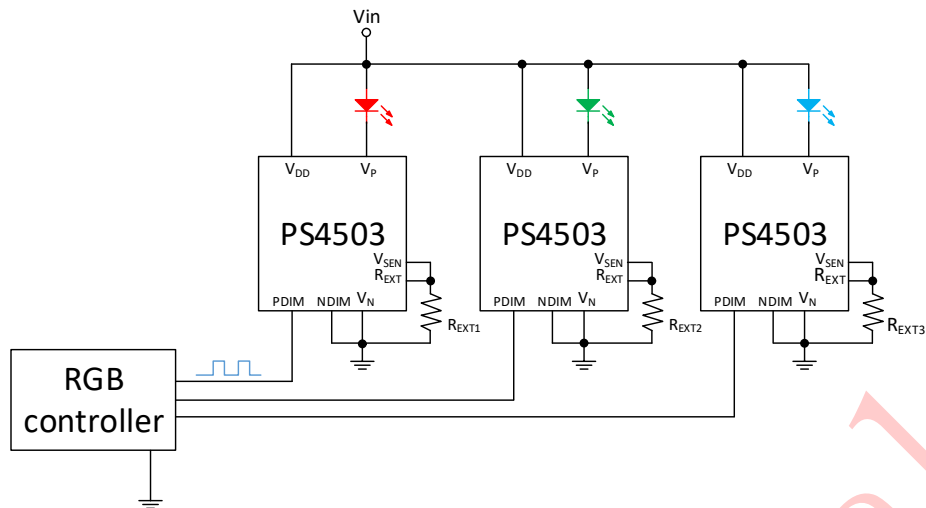


Figure 15. Controller driving current expansion for decoration lighting application.

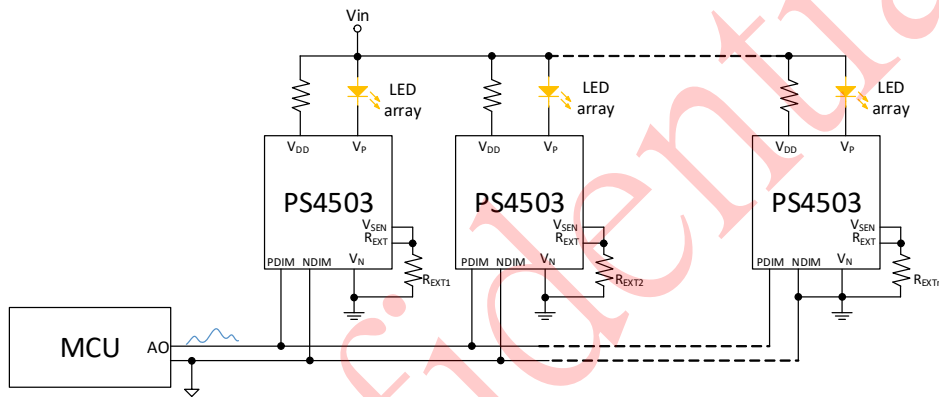
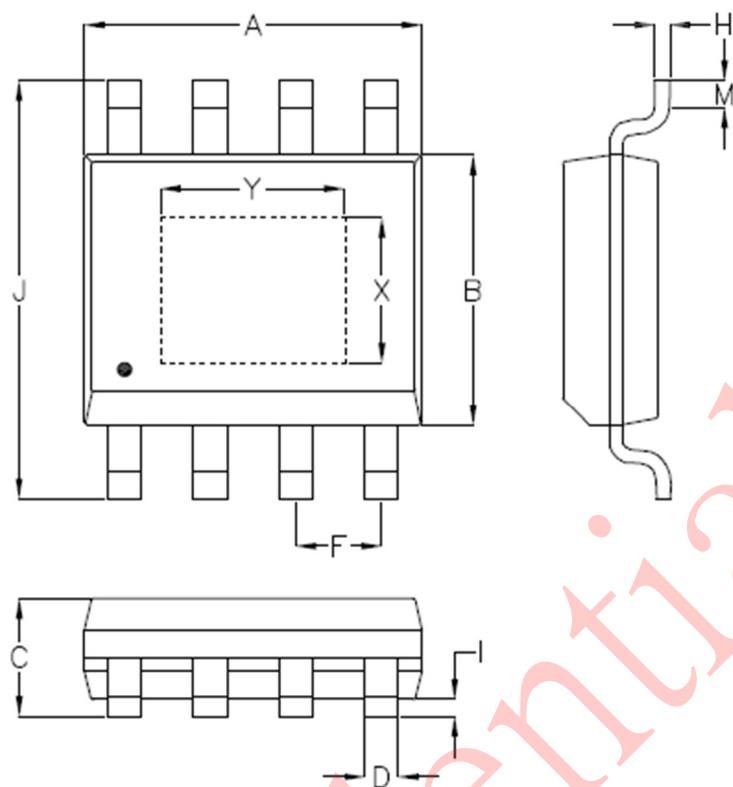


Figure 16. Driving current expansion for wide area zero flicker lighting application.

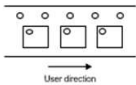
Note: The R_{EXT} resistor should be placed close to the V_{SEN} , R_{EXT} , and GND (V_N) pins. The main purpose is to shorten the trace path between V_{SEN} and GND (V_N) to reduce the impact of noise or voltage drops on current regulation. This layout optimization helps ensure the stability and accuracy of current control.

8 Outline Dimension & Land Pattern

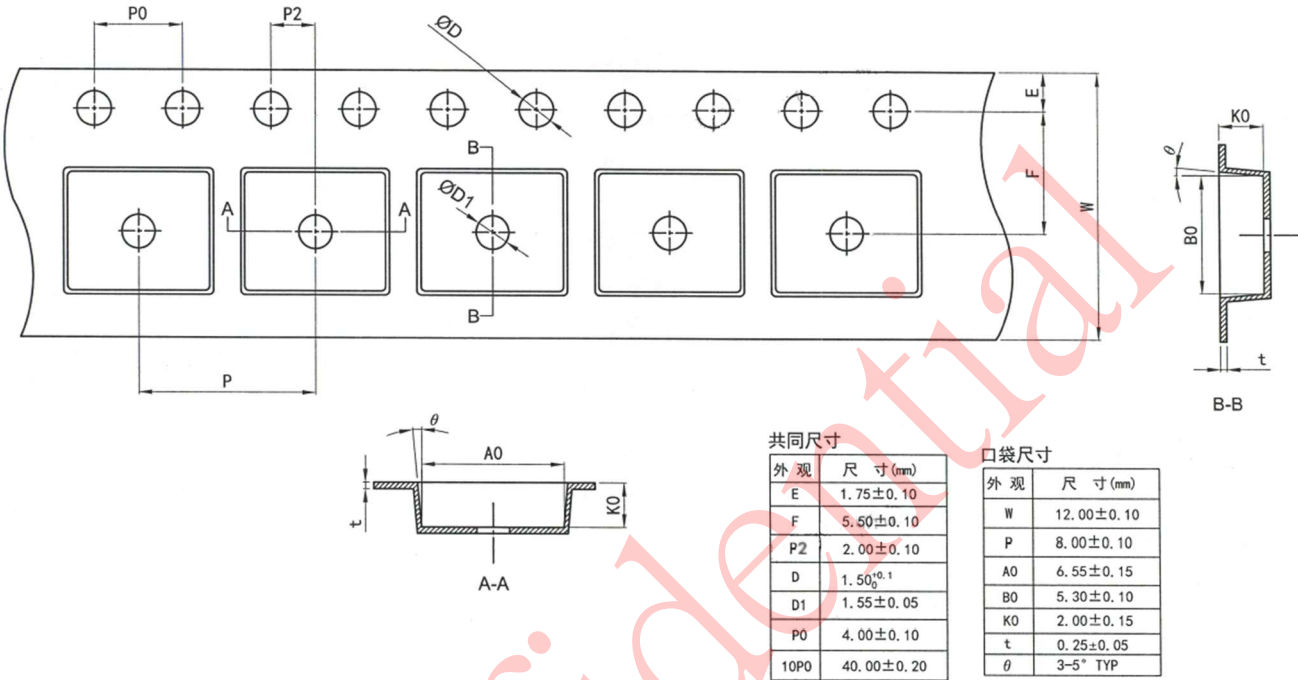


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.801	4.903	5.004	0.189	0.193	0.197
B	3.810	3.905	4.000	0.150	0.154	0.157
C	1.346	1.550	1.753	0.053	0.061	0.069
D	0.330	0.420	0.510	0.013	0.017	0.020
F	1.194	1.270	1.346	0.047	0.050	0.053
H	0.170	0.212	0.254	0.007	0.008	0.010
I	0.000	0.076	0.152	0.000	0.003	0.006
J	5.791	5.996	6.200	0.228	0.236	0.244
M	0.406	0.838	1.270	0.016	0.033	0.050
X	2.100	2.300	2.500	0.083	0.091	0.098
Y	3.000	3.250	3.500	0.118	0.128	0.138

9 Tape & Reel Drawing

封装型態 Package type	軸片直徑 Reel Diameter(inch)	承載帶寬 Carrier width(mm)	承載帶間距 Carrier Pitch(mm)	極性方向 Pin1 Orientation	每捲數量 Units Per Reel	每內盒總數量 TTL QTY Per Inner Box	每外箱總數量 TTL QTY Per Carton
PSOP8	13	12	8		3,000	3,000	18,000

Note: greater than 16cm on the trailer and greater than 60cm on the leader.



10 Restrictions on product use

- PowerX Semiconductor reserves the right to update these specifications in the future.
- The information contained herein is subject to change without notice.
- PowerX Semiconductor will continually be working to improve the quality and reliability of its products. Nevertheless, semiconductor device in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress.

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